REMARKS

These amendments and remarks are in response to the Office Action dated May 3, 2005. Claims 1-38 are pending in the application.

In the Office Action, the Examiner rejected claims 1, 20, and 37 under 35 U.S.C. § 112, second paragraph as failing to comply with the enablement requirement. Claims 1-38 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite. Further claims 1-38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,285,679 B1 ("Dally") in view of U.S. Patent No. 6,285,679 B1 ("Irwin").

Each of the rejections from the Office Action of May 3, 2005 is discussed below in connection with the various claims. Further, with this response, Claims 1, 11, 20, 30, 31, 36, 37 and 38 have been amended to clarify the claims and have not been amended for the purpose of patentability. In addition, new claims 39-41 have been added. No new matter has been added. Reconsideration of the application is respectfully requested in light of the following amendments and remarks.

I. REJECTIONS UNDER 35 U.S.C. § 112

A. Rejection of Claims 1, 20, and 37 Under 35 U.S.C. § 112, first paragraph

Claims 1, 20, and 37 were rejected under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. Specifically, the Examiner asserted that, given the "well-known understanding in the art of digital designs requir[ing] the use of states, it is unknown ... how a processor (i.e. microprocessor) is able to be stateless."

With this response, claims 1, 20, and 37 have been amended for clarity. Applicants submit the specification along with the amended claims meet the enablement requirement of 35 U.S.C. § 112, first paragraph. Support for these amendments may be found at least at paragraph [0181] in the specification (paragraph [0189] as published). Therefore, Applicants request that the Examiner withdraw this rejection of these claims.

B. Rejection of Claims 1-38, Under 35 U.S.C. § 112, second paragraph

Claims 1-38 were rejected under 35 U.S.C. § 112, second paragraph, as indefinite. Specifically, the examiner asserted that "the current claims are broad and general to the point of failing to truly detail the functions being performed."

The Examiner further asserted that "no details are claimed for what is being filtered, or how the filtering is performed, or what incentives are offered" and that "no details are claimed regarding how the packets are selected and what process is performed on the selected packets." With this response, claims 1, 11, 20, 30, 37, and 38 have been amended for clarity. Support for these amendments may be found at least at paragraphs [0117] and [0184] of the specification (paragraphs [0125] and [0192], respectively, as published).

The Examiner also asserted that the claims contain a "description of processor placement/layout within the design without claiming what incentives such placement/layout offers." Applicants are not aware of any statutory requirement to claim what incentives are offered. "[A]pparatus claims cover what a device *is*, not what a device *does*." MPEP § 2114 citing *Hewlett-Packard Co. v. Bausch & Lomb Inc.*, 909 F.2d 1464, 1469 (Fed. Cir. 1990) (emphasis in original). As required by 35 U.S.C. § 112, Applicants have particularly pointed out and distinctly claimed the subject matter which they regard as their invention. Nonetheless, one of ordinary skill in the art would appreciate that the claimed parallel arrangement distributes the incoming workload among the associated processors while the claimed serial arrangement distributes the task processing among the associated processors, which in either case reduces the workload on, and increases the throughput of, any given processor so arranged.

Applicants therefore request that the Examiner withdraw this rejection of these claims.

II. REJECTIONS UNDER 35 U.S.C. § 103(a)

A. Claim 1, 20, 37 and 38

Claims 1, 20, 37 and 38 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Dally in view of Irwin. Applicants submit that claims 1, 20, 37 and 38 should be allowed because Dally, alone or in combination with Irwin, fails to disclose all of the elements of these claims.

Dally discloses:

> A router routes data packets. The router includes input physical channels for incrementally receiving portions of the data packets, and output physical channels. The router further includes data buffers, coupled with the input and output physical channels, for storing the portions of the data packets. The router further includes control circuitry, coupled with the input and output physical channels and the data buffers, for generating virtual channel assignments that assign virtual channels to the data packets, and generating physical channel assignments that assign the output physical channels to the virtual channels. Each of the assignments is generated in response to queued arrival and credit events. The portions of the data packets are forwarded from the data buffers to the output physical channels according to the generate virtual and physical channel assignments.

See Dally Abstract.

Irwin discloses:

> A data packet processing system is provided for a router having a multiprocessor architecture comprising a master node and a processor array of multiple slave nodes. A packet switching software of the router is partitioned into a main forwarding program which is loaded in the master node, and a set of procedures which is loaded into the slave nodes. The system assigns to each data packet a program counter which defines a sequence of procedural calls in the main forwarding program. By stepping through the program counter in the master node, each procedural call is forwarded to and executed by one of the slave nodes.

See Irwin Abstract.

Neither Dally nor Irwin, taken alone or in combination, disclose all of the limitations of independent claims 1, 20, 37 and 38. In particular, the Examiner admits that "Dally's disclosure does not detail the number of processors within the router." Office Action, May 3, 2005, page 5. Applicants submit that it is implicit in this admission that Dally cannot disclose the arrangement or function of processors without disclosing the number of processors.

Irwin does allow for multiple processors, however the processors in Irwin are not arranged as claimed in the limitations set forth in claims 1, 20, and 37. Specifically, Irwin fails to disclose "two ... processors coupled in parallel with each other" along with "two ... processors coupled in series with each other" or "performing ... processing in parallel by ...

two ... processors" along with "receiving ... packets from said first secondary packet processor by a second secondary packet processor" or "parallel processing means" along with "serial processing means" as claimed in claims 1, 20, and 37 respectively. Instead, the arrangement of processors in Irwin is disclosed as a ring or cluster topology. Irwin Fig. 7 and Fig. 22.

In addition, Irwin fails to disclose the tasks each processor is operative to perform as claimed in claims 1, 20, 37, and 38. Specifically, Irwin fails to disclose a "primary processor ... operative to perform stateless processing tasks" along with a "secondary processor ... operative to perform stateful processing tasks" or "at least two ... processors each operative to perform stateless processing tasks" along with a "processor operative to perform a first stateful packet processing task" or a "means for performing stateless processing tasks" along with a "means for performing stateful processing tasks" or a "processor ... operative to monitor said intercepted packets for predefined conditions and at least one of delete, modify, and log packets which meet said pre-defined conditions" as claimed in claims 1, 20, 37, and 38 respectively. In Irwin, "rather than dedicating a processor to a single data packet, the data packet processing is distributed to the processor array." Irwin, Col. 5 lines 44-46. Further, while Irwin teaches "multithreaded parallel processing capability," Irwin fails to teach performing stateful processing tasks or a processor which is operative to monitor intercepted packets for predefined conditions and take one of the claimed actions as required by the claims. Irwin, Col. 7 lines 18-19.

Accordingly, as both Dally and Irwin fail to disclose all of the limitations of independent claims 1, 20, 37, or 38, the combination of these references also does not disclose all of the elements of these claims. For at least the reasons stated above Applicants respectfully request the withdrawal of the rejection to Claims 1, 20, 37 and 38 under 35 U.S.C. § 103(a).

B. Dependent Claims 2-19 and 21-36

Dependent claims 2-19 and 21-36 were also rejected under 35 U.S.C. § 103(a) as being unpatentable over Dally in view of Irwin. Claims 2-19 are dependent on independent claim 1 and claims 21-36 are dependent on independent claim 20. As explained above, Dally, alone or in combination with Irwin, does not disclose all of the elements of claim 1 or

20. Accordingly, Dally in combination with Irwin does not disclose all of the elements of claims 2-19 and 21-36. Therefore, Applicants respectfully request the withdrawal of the rejection to claims 2-19 and 21-36 under 35 U.S.C. § 103(a).

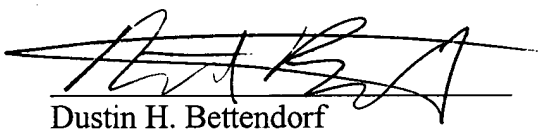
III. NEW CLAIMS

With this response, new claims 39-41 have been added. Support for these claims may be found in the specification. No new matter has been added. New claims 39-41 should be allowed over the cited references for the same reasons as discussed above. Accordingly, Applicants request that the Examiner allow new claims 39-41.

CONCLUSION

In view of the foregoing remarks and amendments, Applicants submit that the pending claims and new claims are in condition for allowance. Reconsideration is therefore respectfully requested. If there are any questions concerning this response, the Examiner is asked to phone the undersigned attorney at (312)-321-4200.

Respectfully submitted,



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